submitted that the present title is clearly indicative of the invention to which the claims are directed.

The Office Action also asserts that the Abstract is not in proper format. Applicants respectfully submit that the Abstract has been amended according to the Examiner's recommendations.

Claims 1, 4-9 and 12 have been amended for clarity and to further define the subject matter Applicants regard as the invention. Claim 3 has been canceled without prejudice to or disclaimer of the subject matter contained therein. Claims 2, 10, 11 and 13 remain unchanged. Thus, claims 1, 2 and 4-13 are presently pending in this application for consideration.

Applicants respectfully submit that the pending claims are patentably distinguishable over the cited references as required by § 102 and §103. Applicants further submit that the cited references, whether taken alone or in any combination, fail to disclose the first dummy pattern and the second dummy pattern formed initially within the dicing region as recited in independent claim 1. Thus, claim 1 and all claims dependent therefrom are allowable over the cited references. This distinction will be further described in the following section.

THE CLAIMS DISTINGUISH OVER THE CITED REFERENCES

Claims 1-3 and 8-13 stand rejected under 35 U.S.C. 102(a) as being anticipated by Yamaha. Claims 4 and 5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha in view AAPA and claims 6 and 7 stand rejected under the same as being unpatentable over Yamaha in view of Morita. These rejections are respectfully traversed since independent claim 1 includes the feature of the first dummy pattern and the second dummy pattern formed initially within the dicing region. This claimed feature is not disclosed or suggested in the cited references.

The present invention is directed to a semiconductor device formed by using a dicing technique for separating semiconductor wafers into chips. According to one embodiment of the present invention and as illustrated in Fig. 8, a semiconductor wafer is provided with both first dummy patterns 18 and second dummy patterns 41 formed on a dicing line 2. A plurality of element isolation regions 12 and the plurality of first dummy patterns 18 are arranged alternately in a repetitive pattern in a region corresponding to the dicing line 2. The plurality of second

dummy patterns 41 are provided to correspond respectively to the first dummy patterns. With this arrangement, the size of a crack cause during a dicing operation can be reduced.

Yamaha is directed to a semiconductor chip capable of suppressing cracks in an insulating layer. The Examiner alleges that Yamaha discloses a semiconductor device having a plurality of first dummy patterns $4b_1$ formed on the surface of the substrate within the dicing region and a plurality of second dummy patterns 5b formed above the substrate within the dicing region so as to correspond to the plurality of first dummy patterns $4b_1$. However, the first dummy patterns $4b_1$ and the second dummy patterns 5b of Yamaha are not formed, initially, within the dicing region as recited in independent claim 1 (see, for example, Yamaha, column 6, lines 53-55). These semiconductor devices are arranged in totally different ways. Thus, Yamaha fails to disclose the first dummy pattern and the second dummy pattern formed initially within the dicing region as claimed. Moreover, there is no teaching or suggestion of this claimed arrangement. Neither AAPA nor Morita disclose this feature and were not cited for that purpose.

In view of the absence of the above claimed feature, the cited references cannot be said to anticipate and do not render obvious the apparatus defined by claim 1. Moreover, since claim 1 is allowable, the claims dependent therefrom, namely claims 2 and 4-13 are also allowable. Further remarks regarding the asserted relationship between these claims and the cited references are not necessary in view of their allowability. Applicants' silence as to the Examiner's comments is not indicative of an acquiescence to the stated grounds of rejection.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for all wance. Reexamination and reconsideration f thc application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Washington, D.C. telephone number 202 637-3615 to discuss the steps necessary for placing the application in condition for all wance.

Respectfully submitted,

HOGAN & HARTSON, LLP

Date February 5, 2003

By: _____

Sterlon R. Mason
Registration No. 41,179
Attorney for Applicant(s)

Biltmore Tower, Suite 1900
500 South Grand Avenue
Los Angeles, California 90071
Telephone: 213-337-6700
Facsimile: 213-337-6701
psteinpres/81790.0227.rca

Version with markings to show changes made:

IN THE ABSTRACT:

Please amend the original Abstract of the Disclosure as indicated below.

[In manufacturing a semiconductor memory, a gate oxide film, a polysilicon film and a WSi film are laminated on the major surface of a semiconductor wafer corresponding to both an element region on which a semiconductor chip is to be formed and a dicing region serving as a dicing line. These laminated films are patterned to form a projected dummy pattern having substantially the same wiring structure as that of a gate electrode portion of a selective transistor. The dummy pattern is formed between element isolation regions along a dicing direction at the same time when the gate electrode portion is formed. The dummy pattern prevents stress caused by dicing from being concentrated on an insulation film in the dicing region, thereby minimizing a crack waste. Consequently, in the semiconductor memory, a malfunction due to a large crack waste caused by the dicing, can be avoided.]

A semiconductor device includes a dicing region provided on a semiconductor substrate to separate a plurality of semiconductor chips each having a gate portion from each other. The semiconductor device further includes a plurality of element isolation regions provided on a surface portion of the semiconductor substrate within the dicing region, a plurality of first dummy patterns formed on a surface of the semiconductor substrate so as to correspond to intervals of the plurality of element isolation regions, respectively, and a plurality of second dummy patterns formed above the semiconductor substrate within the dicing region so as to correspond to the plurality of first dummy patterns, respectively.

IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Once Amended) A semiconductor device comprising:

a dicing region provided on a semiconductor substrate to separate a plurality of semiconductor chips each having a gate portion from each other;

a plurality of element isolation regions provided on a surface portion of the semiconductor substrate within the dicing region;

a plurality of first dummy patterns formed on a surface of the semiconductor substrate [within the dicing region] so as to correspond to intervals of the plurality of element isolation regions, respectively; and

a plurality of second dummy patterns formed above the semiconductor substrate within the dicing region so as to correspond to the plurality of first dummy [patters] patterns, respectively.

4. (Once Amended) The semiconductor device according to claim [3] 1, wherein the plurality of first dummy patterns each have a structure which is substantially similar to that of the gate potion.

5. (Once Amended) The semiconductor device according to claim 4, wherein the plurality of first dummy patterns and the gate portions each have a laminated structure including a gate oxide film, a polysilicon film, a WSi film, and a SiN film.

6. (Once Amended) The semiconductor device according to claim 1, wherein the plurality of element isolation regions [having] each have an STI structure [is formed by each side of the plurality of first dummy patterns].

7. (Once Amended) The semiconductor device according to claim [5] 1, wherein the plurality of first dummy patterns and the element isolation regions are arranged alternately to form a predetermined repetitive pattern.

8. (Once Amended) The semiconductor device according to claim 1, wherein the plurality of second dummy patterns [are] include at least protection films provided on the surface of the semiconductor substrate.

9. (Once Amended) The semiconductor device according to claim [1] 8, wherein the plurality of second dummy patterns include insulation films [deposited] provided on the surface of the semiconductor substrate.

12. (Once Amended) The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the plurality of second dummy patterns are formed along [a dicing direction of] the dicing region.